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| EWULogo.png | | **EAST WEST UNIVERSITY** | |
| **Department of Computer Science and Engineering** | |
| **B.Sc. in Computer Science and Engineering Program** | |
| **Mid Term II Examination, Spring 2019** | |
| **Course:** | | **CSE442 – Microprocessors and Microcontrollers, Section-1** |  |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Associate Professor, CSE Department** |  |
| **Full Marks:** | | **20 (15 mark will be counted for final grading)** |  |
| **Time:** | | **1 Hour and 20 Minutes** |  |
| **Note:** There are FIVE questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin. | | | |
| 1. | Design a ROM chip with all control signals having 128 KB of memory location. | | [CO1, C3, 3] |
| 2. | Design an interface between a memory 27512EPROM and Intel 8088 microprocessor using a NAND gate decoder. Calculate the memory location decoded by NAND gate. Determine the output of the NAND gate and show the inputs of the control signals for reading data. | | [ CO1, C3, 5] |
| 3. | Analyze the diagram and determine the LED lights that will be glown by the given configuration of the toggle switches in Figure 1. Write the assembly language program for the output. Draw the output. | | [ CO2, C3, 4] |
|  | **Figure 1. 7- Segment display** | |  |
| 4 | Design an address multiplexer for DRAM that contains only 16 address inputs, where it should contain 32-the numbered required addressing 4GB memory locations. Determines the pins functions for the operations. | | [ CO2, C3, 3 ] |
| 5. | Analyze the clock generator 8284A for 8086/8088 microprocessor given in Figure 2. Determine the output for the following operations in a tabular form as indicated below.   1. When F/C=0 2. When F/C=1  |  |  |  |  | | --- | --- | --- | --- | |  | **CLK** | **PCLK** | **OSC** | | a) |  |  |  | | b) |  |  |  |     **120 MHz** | | [CO2, C3, 5] |
| 6. | |  |  | | --- | --- | | Generate the Vector Number from (Figure-1) and calculate the corresponding ISR address (from Table 1) in real mode 8088 processor | | | Figure 3. 8-bits interrupt number generator circuit. | Table-1: Interrupt Vector Table   |  |  | | --- | --- | | Vector# | Addresses (Segment & Offset) | | 80H | 87H | | …… | …… | | 37H | 5DH | | 36H | 23H | | 35H | FEH | | 34H | 12H | | 33H | F1H | | 32H | 4CH | | 31H | 40H | | 30H | 10H | | …. | ….. | | 1FH | 1CH | | 1EH | 1AH | | 1DH | 10H | | 1CH | 12H | | | |  |